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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,405	10/08/2003	David R. Welland	SILA:035C2	7435

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EXAMINER	
GESESSE, TILAHUN	
ART UNIT	**PAPER NUMBER**
2684	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,405	WELLAND ET AL.	
	Examiner	Art Unit	
	Tilahun B Gesessse	2684	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *1 and 2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/8/03 and 11/24/*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 3-26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-39 of U.S. Patent No. 6,741,846. Although the conflicting claims are not identical, they are not patentably distinct from each other because all limitations claimed in the present application are claimed in the patented reference, such as, claim 1, of the indicated patent. Therefore, it is proper to reject claims 3-26 under obviousness-type double patenting as being unpatentable over claims 1-39 of 6,741,846.

Claim Rejections - 35 USC § 102

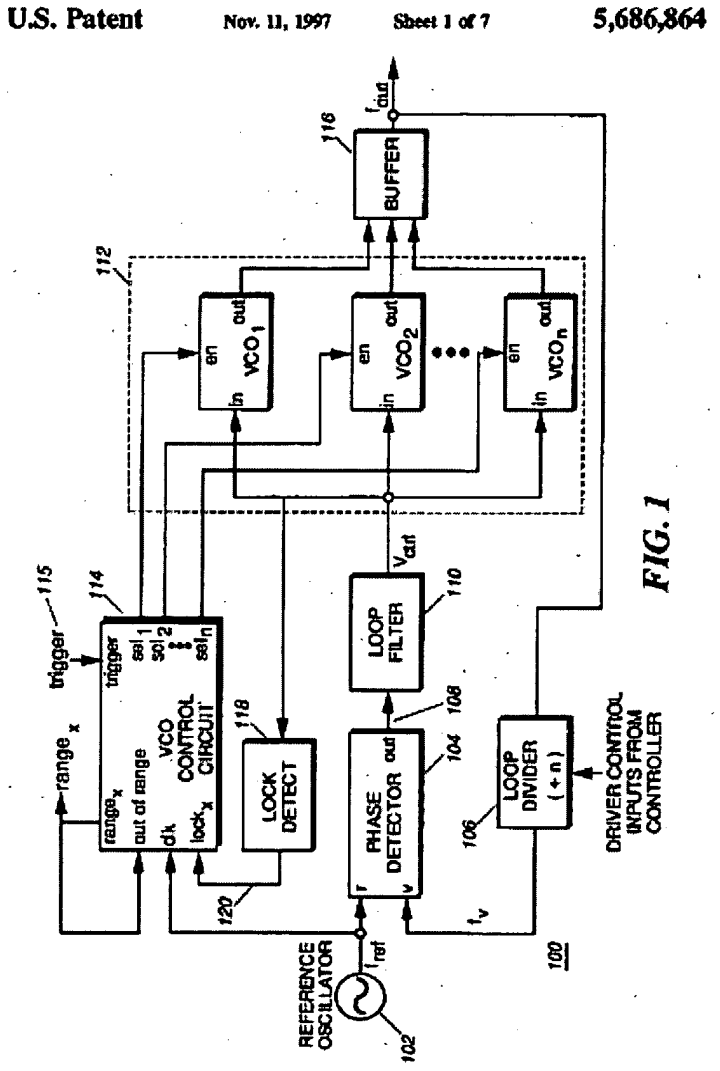
3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 12,14-20,22-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Martin et al (US 5,686,864).

Claim 12, Martin discloses phase locked loop circuitry (104) for generating an output signal at a variable output frequency (figure 1 and 5), a controllable oscillator (112,502) having an output signal at an output frequency dependent upon a plurality of different analog control signals, the plurality of different analog control signals being received by the controllable oscillator as different frequency control input signals such that at least some of the plurality of control signals are configured to individually control the controllable oscillator without being combined with others of the plurality of control signals ((see column 1 line 63-column 3, line 30 and column 5, line 42-column 6, line 8 and figures 1 and 5) and phase difference control circuitry configured to concurrently provide the plurality of different analog control signals as outputs, the plurality of different analog control signals being generated from a phase difference between at least two input signals ((see figures 1 and 5 and column 1 line 68-column 2 line 20), wherein the controllable oscillator comprises a plurality of non-varactor diode capacitance circuits connected in parallel to contribute a combined capacitance amount that determines at least in part the output frequency of the controllable oscillator, the

plurality of different analog control signals from the phase difference control circuitry being coupled to control the amount of capacitance contributed by the plurality of capacitance circuits (column 5, line 59-column 6, line 8 and figure 6).



Claims 14,22 Martin discloses the controllable oscillator comprises an LC tank resonant structure including the plurality of capacitance circuits(column 5, lines 59-column 6, line 8 and figure 6).

Claims 15,23 Martin discloses the each of the plurality of capacitance circuits comprises at least one capacitor and a variable resistance element, the variable resistance element being coupled to at least one of the plurality of analog control signals.(column 5,line 59-column 6, line 8, and figure 6)

Claims 16,24 Martin discloses the variable resistance element comprises a transistor and wherein at least one capacitor is coupled to the source or drain of the transistor and the control signal is coupled to the gate of the transistor (column 5, line59-column 6, line 8 and figure 6).

Claims1 7,25 Martin discloses at least a second capacitor coupled between the source and drain of the transistor (column 5, line 59-column 6, line 8 and figure 6).

Claim 18, Martin discloses at least one of the input signals to the phase difference control circuitry is adjustable and is configured to determine at least in part the frequency of the output signal (figures 1 and 5).

Claims 19,26Martin discloses one input signal to the phase difference control circuitry is an adjustably divided version of the output signal and a second input signal to the phase difference control circuitry is an adjustably divided version of a reference signal, the first and second (figures 1 and 5)

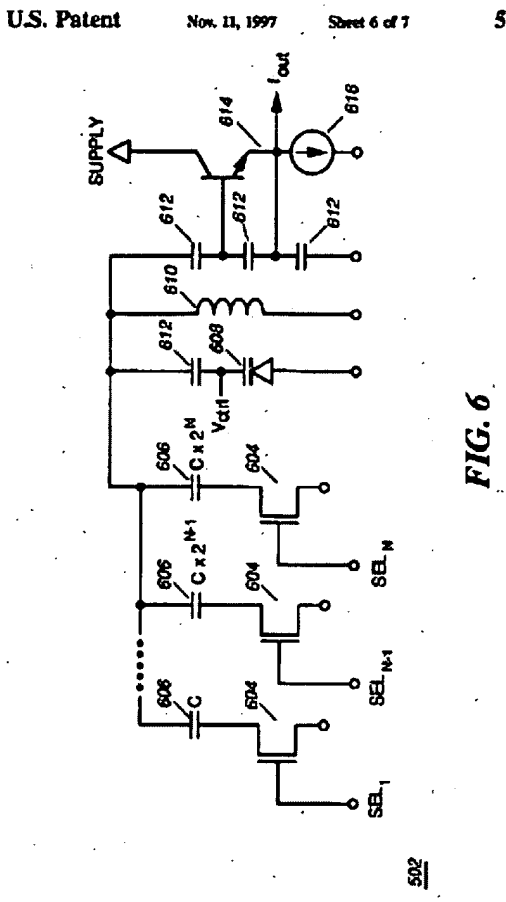


FIG. 6

Claim 20, it recites features which corresponds to claim 12 above. Therefore, it is analyzed and rejected for the same reason as set forth in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-11, 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al "Martin" (US 5,686,864) in view of Borras et al "Borras" (US 4,484,153).

Claims 3,13, and 21 Martin discloses a frequency synthesizer having a phase locked loop (100,500 of figures 1 and 5, a controllable oscillator (112,502 VCOs) having an output frequency dependent upon a plurality of control signals (outputted from controller 114), the plurality of control signals being received by the controllable oscillator as frequency control input signals and are configured without being combined with other plurality of control signals (see column 1 line 63-column 3, line 30 and column 5, line 42-column 6, line 8 and figures 1 and 5). Martin discloses a phase detector configured to concurrently provide a plurality of different analog output signals, the plurality of different analog output signals being generated from a phase difference between at least two input signals (fref and fv) (see figures 1 and 5 and column 1 line 68-column 2 line 20).

Martin differs in teaching a sample and hold circuit coupled to sample each of the different plurality analog output signals from the phase detector and to hold a plurality of different sampled analog output signals, the different sampled analog output signals being used to provide the plurality of different control signals for the controllable oscillator. However, Borras discloses a sample and hold circuit coupled to sample each of the different plurality analog output signals from the phase detector and to hold a plurality of different sampled analog output signals, the different sampled analog output signals being used to provide the plurality of different control signals for the controllable

oscillator (column 4, lines 7-16 and column 4, line 66-column 5, line 11and figure 2). Since, Martin, in similar field of endeavor, teaches sampling technique (column 4, lines 42-60 and figure 3), then, It would have been obvious to ordinary skill in the art at the time of invention was made to sample and hold to provide control analog signals from the phase detector to the controllable oscillator in order to monitor the phase difference signal and locks the desired signal.

As to claim 4,Martin discloses input signals to the phase detector (104) comprising a first input signal coupled to an output of the controllable oscillator and a second input signal coupled to a reference signal (see figures 1 and 5, fv and fref).

As to claim 5, Martin discloses as explained in claim 4, a phase detector (104)) having a plurality of analog output signals, the analog output signals being between at least two input signals (figures 1 and 5).

Claims 6-8,Martin substantially discloses the number of first input signals and the number of analog output signals is equal (figures 1 and 5) and the number of analog output signals is at least five (at least five see figures 1 and 5), the number of analog output signals is at least twenty (see figures 1 and 5).

Claim 9, Martin discloses the plurality of first input signals are signals having at least one phase shifted edge with respect to each other (column 4 lines 42-60)

Claim 10, Martin discloses a shift register having the plurality of phase-shifted signals as outputs (figure 2 and it's disclosure).

Claim 11, Martin discloses detector (104) comprises a plurality of phase detector sub-circuits, each sub-circuit having as an output one of the plurality of analog output

signals and having as inputs at least one of the plurality of first signals and at least one of the second signals (figures 1 and 5).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Leblebicioglu (5,369,376) discloses programmable phase locked loop circuit (see abstract and figures 1-5).

Maddy et al (US 5,334,952) discloses a phase locked loop including a switch between phase detector output and a VCO and PLL (abstract).

Davis (US 4,893,087) discloses frequency synthesizer includes a memory containing information to provide divider information to the variable divider of phase locked loop (abstract).

. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tilahun B Gesesse whose telephone number is 703-308-5873. The examiner can normally be reached on flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 703-308-7745. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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January 5, 2005

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